

IN THE CLAIMS:

1. (Currently Amended) A semiconductor device comprising:  
peripheral electrodes formed on a periphery of a  
semiconductor chip;

internal electrodes formed inside the peripheral electrodes  
on the semiconductor chip; and

circuits formed in the semiconductor chip,

wherein the peripheral electrodes are connected to the  
circuits by an internal line, and the internal electrodes are  
connected to the circuits and the peripheral electrodes by the  
internal line, said internal line being covered by an insulating  
layer, and

wherein a same signal is either an input and/or output  
either to or from both the internal electrode and the peripheral  
electrodes, and

wherein rewiring is connected to either the peripheral  
electrodes, or to the internal electrodes ~~in the case of CSP~~  
~~packaging~~, and a wire is connected to the peripheral electrodes  
~~in the case of~~ connecting to external terminals using wire  
bonding, said peripheral electrodes being formed within an  
opening provided in said insulating layer.

2. (Original) A semiconductor device according to Claim 1, wherein the internal electrodes are smaller than the peripheral electrodes.

3. (Original) A semiconductor device according to Claim 1, wherein the internal electrodes comprise at least one selected from the group consisting of a power supply terminal, a ground terminal, and a clock terminal.

4. (Previously Presented) A semiconductor device according to Claim 1, wherein the peripheral electrodes not connected to the internal electrodes are used as terminals for RF signals.

5. (Currently Amended) A semiconductor device comprising:  
peripheral electrodes formed on a periphery of a  
semiconductor chip;

internal electrodes formed inside the peripheral electrodes  
on the semiconductor chip; and

circuits formed in the semiconductor chip,

wherein the peripheral electrodes are connected to the  
circuits by an internal line covered by an insulating layer, the  
internal electrodes are connected to the circuits and the  
peripheral electrodes by the internal line, and the internal  
electrodes are also connected to rewired lines, the rewired

lines formed above the internal electrodes with an insulating layer therebetween, and at ends of the rewired lines formed area array electrodes, and said peripheral electrodes being formed within openings provided in said insulating layer.

6. (Currently Amended) A semiconductor device comprising:  
peripheral electrodes formed on a periphery of a  
semiconductor chip;

internal electrodes formed inside the peripheral electrodes  
on the semiconductor chip;

area array electrodes connected to selected one of the  
peripheral electrodes and the internal electrodes and formed on  
the semiconductor chip; and

circuits formed in the semiconductor chip,

wherein the peripheral electrodes are connected to the  
circuits by an internal line covered by an insulating layer, the  
internal electrodes are connected to the circuits and the  
peripheral electrodes by the internal line, and the area array  
electrodes comprise first area array electrodes connected to the  
internal electrodes by rewired lines and second area array  
electrodes connected to the peripheral electrodes by rewired  
lines, said peripheral electrodes being formed within openings  
provided in said insulating layer.

7. (Original) A semiconductor device according to Claim 6, wherein the first area array electrodes comprise at least one selected from the group consisting of a power supply terminal, a ground terminal, and a clock terminal.

8. (Previously Presented) A semiconductor device according to Claim 6, wherein the second area array electrodes are used as terminals for RF signals.